WHAT IS CLAIMED IS:

1. A MOSgated device comprising:

a semiconductor substrate of one of the conductivity types and having an upper planar surface;

a channel diffusion region of the other of the conductivity types which extends into said upper planar surface of said substrate and to a first depth below said surface;

a source diffusion of said one of the conductivity types which extends into said substrate to a second depth which is less than said first depth;

a plurality of spaced trenches formed into said substrate and into its said upper planar surface to a third depth below said substrate surface which is greater than said first depth;

an insulation gate layer formed on the walls of said plurality of trenches at least in the areas between said first and second depths;

conductive gate bodies disposed within the interiors of each of said trenches;

a plurality of narrow, spaced conductive gate strips disposed atop said insulation gate layer and extending across and contacting each of said conductive gate bodies;

a source contact connected to said source diffusion region at a location on said upper planar surface which is completely laterally removed from said plurality of trenches;

a gate electrode connected to said plurality of conductive gate strips;

and a drain contact connected to said substrate.

2. The device of claim 1 wherein said plurality of spaced trenches are parallel to one another and are coextensive with one another.

3. The device of claim 2 wherein said plurality of spaced trenches are formed in a plurality of spaced rows and are parallel to one another and are coextensive with one another within each row.

4. The device of claim 1 wherein said trenches have a depth of about 1.8 microns.

5. The device of claim 1 wherein said third depth is about 0.2 to 0.25 microns deeper than said first depth.

6. The device of claim 4 wherein said third depth is about 0.2 to 0.25 microns deeper than said first depth.

7. The device of claim 1 wherein said trenches have a width of about 0.6 microns and a spacing of about 0.6 microns or greater.

8. The device of claim 4 wherein said trenches have a width of about 0.6 microns and a spacing of about 0.6 microns or greater.

9. The device of claim 5 wherein said trenches have a width of about 0.6 microns and a spacing of about 0.6 microns or greater.

10. The device of claim 1 wherein said gate insulation is an oxide layer having a thickness greater than about 200 Å and which fully covers the interior of each of said trenches and wherein each said conductive gate bodies is polysilicon which completely fills each of said trenches and is insulated from said substrate.

11. The device of claim 1 wherein said source contact is further connected to said channel region as well as said source region.

12. In a MOSgated device; a semiconductor substrate of one of the conductivity types and having an upper surface; at least first and second invertible vertical channel forming trenches formed through said upper surface and into said substrate for a first depth; a gate oxide coating the interior walls of said at least first and second trenches; a channel region of the other conductivity type disposed adjacent to a portion of the length the walls of said first and second trenches and to a second depth below said upper surface, said second depth being less than said first depth; a shallow source region which extends from said upper surface and into said substrate for a third depth; said third depth being less than said second depth; first and second spaced conductive polysilicon layers filling said at least first and second trenches respectively and which are insulated from said substrate; and at least one narrow conductive polysilicon gate strip disposed atop and insulated from said upper surface and extending across and contacting each of said first and second spaced conductive polysilicon layers.

13. The device of claim 12 which further includes a source contact which is fully laterally spaced from the area of said upper surface which is between said

at least first and second trenches and connected to at least said source region at a location remote from said first and second trenches.

14. The device of claim 13 in which said source contact is also connected to said channel region at said remote location.

15. The device of claim 12 wherein said trenches have a depth of about 1.8 microns.

16. The device of claim 12 wherein said channel region is about 0.2 to 0.25 microns deeper than said trenches.

17. The device of claim 16 wherein said trenches have a depth of about 1.8 microns.

18. The device of claim 12 wherein said trenches have a width of about 0.6 microns and a spacing of about 0.6 microns or greater.

19. The device of claim 15 wherein said trenches have a width of about 0.6 microns and a spacing of about 0.6 microns or greater.

20. The device of claim 18 in which said source contact is also connected to said channel region at said remote location.

21. A process for the manufacture of a MOSgated power device; said process comprising the steps of diffusing a channel region of one conductivity type into a surface of a substrate of the other conductivity type to a first depth; diffusing a source region of the other conductivity type to a second depth which is less than said first depth; etching a plurality of spaced and generally U-shaped trenches into the surface of said silicon substrate to a third depth which is greater than said first depth; forming a gate oxide over the interior surfaces of said trenches and forming an insulation oxide over the surface areas between said trenches; and then depositing a continuous layer of conductive polysilicon into each of said trenches and over said insulated surface between said trenches; and then etching away a portion of the layer of polysilicon, leaving at least one narrow strip which extends across and connects the polysilicon in each of said trenches; and forming a source contact to at least said source region at a location laterally removed from the space between said trenches.